

# ECE 5460/6460

## VLSI Design Automation

**Description:** This course will introduce students to basic algorithms and methodologies used for automating the design of modern VLSI circuits. Emphasis will be given on physical design problems including partitioning, floorplanning, placement and routing of VLSI circuits. Students will get experience in the development of VLSI-CAD tools. This course will also focus on some of today's nanometer digital integrated circuit design challenges and how current design automation tools can adapt to address nano-scale VLSI issues.

**Instructor:** Dr. Sanghamitra Roy

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**Lectures:** TR 1.30pm-2.45pm, EL 109

**Office hours:** T 3.00pm-4.00pm (or by appointment)

**Prerequisites:** ECE 2700 or basic familiarity with digital logic design. Knowledge of C/C++ programming languages, algorithms and data structures (CS1400).

**Textbook:** S. Sait, H. Youssef, *VLSI Physical Design Automation: Theory and Practice*, World Scientific, 1999.

**Bring to lectures:** Please bring scrap paper or a notebook to your lectures. We will be working on several short in-class exercises during lectures.

## References (Optional):

- Naveed A. Sherwani, **Algorithms for VLSI Physical Design Automation**, Kluwer Academic Publishers, 1999.
- Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest, Clifford Stein, **Introduction to Algorithms**, 2nd ed., 2001, MIT Press; ISBN: 0262032937.
- Bjarne Stroustrup, **The C++ Programming Language**, 3rd ed., 2000, Addison-Wesley Pub Co; ISBN: 0201700735.
- Nicolai Josuttis, **The C++ Standard Library**, 1st ed., 1999, Addison-Wesley Pub Co; ISBN: 0201379260.
- Selected material from recent publications.

**Learning Objectives:** By the end of the course, you should be able to do the following things:

- Formulate CAD design problems using algorithmic paradigms like simulated annealing, dynamic programming, and mathematical programming.
- Develop and implement CAD algorithms using computer programming.
- Explain why some problems can only be approximately solved after long computations while others are exactly solved in a short time.

## Course Webpage:

<https://spaces.usu.edu/display/usuece5460/ECE+5460+6460+VLSI+Design+Automation>

**Homework:** There will be homework assignments given every one to two weeks to help understand the concepts. Many of the homework assignments will involve programming in C/C++.

**Computer Use:** This course will involve several programming assignments to be done in C/C++ during the course of the semester. Students are expected to work 6 to 8 hours per week on the assignments. The VLSI Design Automation Lab EL 105 is reserved on Wednesday afternoons 12.30-4.30pm

for this class. You can use the lab at other times also if available, or by remote login. If you do not have accounts, please contact Scott Kimber to have accounts. You are welcome to use other machines for the assignments if that's more convenient.

**Exams:** There will be one midterm and a final exam. The exams will be open book and calculators will be allowed. Hand-held computers (PDAs) or laptops are not allowed.

**Grading:** The following weights will be used:

Homework: 45%

Midterm: 25%

Final exam: 25%

Class participation: 5%

Grading is based on a conventional fixed scale:

A: 90-100%

A-: 85-89%

B+: 80-84%

B: 70-79%

B-: 65-69%

C+: 60-64%

C: 55-59%

C-: 50-54%

D+: 47-49%

D: 44-46%

D-: 40-43%

F: 0-39%

The instructor reserves the right to curve up the scores at the end of the semester.

**Late policy:** Late submissions will not be accepted without prior approval by the instructor.

**Disabilities:** In cooperation with the Disability Resource Center, reasonable accommodation will be provided for qualified students with disabilities. Please meet with the instructor during the first week of class to discuss possible arrangements.

**Cheating:** Cheating or plagiarism is not permitted. The instructor reserves the right to fail any student who is caught cheating.

**Course Outline:** The following topics will be covered with some variations:

- Overview of VLSI design flow, styles
- Basics of MOS devices
- Algorithms and data structures
  - Computational Complexity, Big-O notation
  - NP-Completeness, Graph theory and data structures
- Circuit Partitioning
  - Kernighan-Lin algorithm
  - Fiduccia-Mattheyses algorithm
- Floorplanning
  - Representation using Normalized Polish Expression
  - Simulated Annealing algorithm
  - Floorplanning using mathematical programming
- Placement
  - Simulated Annealing algorithm
  - Force directed Placement
  - Partitioning based Placement
  - Min-Cut Placement, Terminal propagation
- Routing
  - Global Routing: Steiner Trees
  - Global Routing: Lee's algorithm
  - Global routing: Soukup's, Hadlock's algorithm
  - Channel routing: Left-edge algorithm
  - Channel routing : VCG and HCG
  - Channel routing : Constrained left-edge, Dogleg algorithm
- Trends in nano-scale IC design, transistor scaling

In addition, the following topics will be covered if time permits:

- Power modeling and optimization
  - Dynamic and leakage power basics
  - Dynamic power reduction techniques
  - Leakage reduction: Multiple  $V_t$ , MTCMOS, VTCMOS
- Thermal aware physical design
- Delay modeling and optimization
  - Elmore delay, Static Timing Analysis
  - Buffer insertion: Van Ginneken's algorithm
  - Gate sizing for circuit delay and power optimization
- A brief introduction to 3D IC design