Revision: Monday, November 8, 1993

CY6116A
CY6117A

2K x 8 Static RAM

Features

- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **High speed**
  — 20 ns
- **Low active power**
  — 550 mW
- **Low standby power**
  — 110 mW
- **TTL-compatible inputs and outputs**
- **Capable of withstanding greater than 2001V electrostatic discharge**

Functional Description

The CY6116A and CY6117A are high-performance CMOS static RAMs organized as 2048 words by 8 bits. Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$), and three-state drivers. The CY6116A and CY6117A have an automatic power-down feature, reducing the power consumption by 83% when deselected.

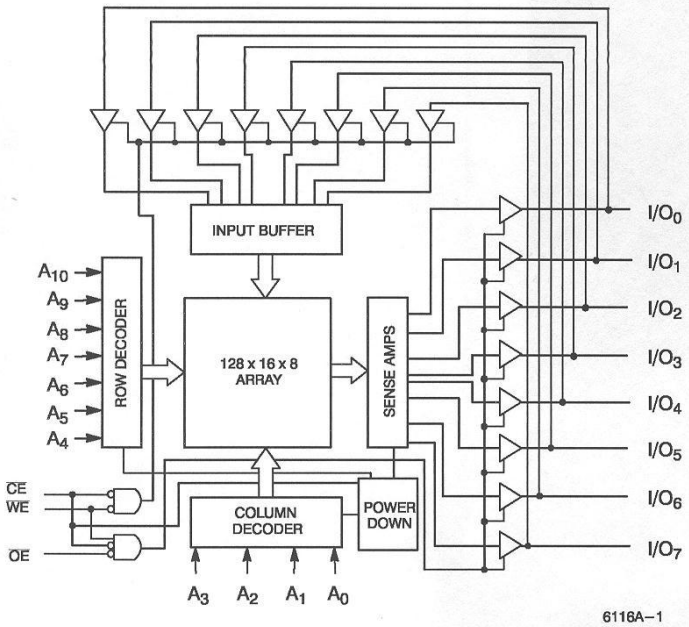
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the I/O pins (I/O_0 through I/O_7) is written into the memory location specified on the address pins (A_0 through A_{10}).

Reading the device is accomplished by taking chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) LOW while write enable ($\overline{WE}$) remains HIGH. Under these conditions, the contents of the memory location specified on the address pins will appear on the I/O pins.

The I/O pins remain in high-impedance state when chip enable ($\overline{CE}$) is HIGH or write enable ($\overline{WE}$) is LOW.

The CY6116A and CY6117A utilize a die coat to insure alpha immunity.

Logic Block Diagram



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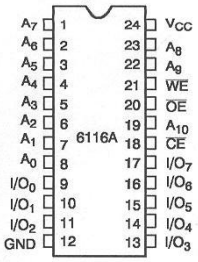
Pin Configurations

DIP/SOJ
Top View



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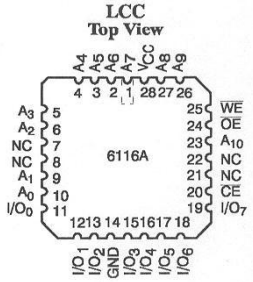
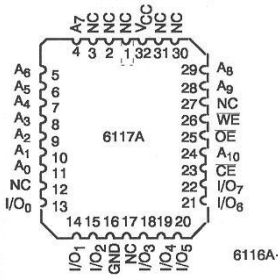
LCC
Top View



6116A–3

LCC
Top View



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Selection Guide

		6116A–20 6117A–20	6116A–25 6117A–25	6116A–35 6117A–35	6116A–45 6117A–45	6116A–55 6117A–55
Maximum Access Time (ns)		20	25	35	45	55
Maximum Operating Current (mA)	Commercial	100	100	100	100	80
	Military		125	100	100	100
Maximum Standby Current (mA)	Commercial	40/20	20	20	20	20
	Military		40	20	20	20