Course Description:
Introduces students to basic algorithms and methodologies used for automating the design of modern VLSI circuits. Emphasizes physical design problems, including partitioning, floorplanning, and placement and routing of VLSI circuits. Students learn to identify and formulate CAD design problems using algorithmic paradigms, such as simulated annealing, dynamic programming, and mathematical programming. Students will also gain experience in the development of VLSI-CAD tools.

Prerequisites:
CS 1400 and ECE 2700

Textbook:

References:


Course Outcomes:
1. Understand the basic algorithms and methodologies for automating the design of modern VLSI circuits.
2. Identify and formulate CAD design problems using algorithmic paradigms like simulated annealing, dynamic programming and mathematical programming.
3. Implement CAD algorithms using computer programming.
4. Understand the functionality and algorithms of the modern VLSI CAD tools and complexity of tool development.
5. Become familiar with the critical challenges in the physical design of nano-scale integrated circuits and how to address these during CAD tool development.

Topics Covered:
- Overview of VLSI design flow, styles
- Basics of MOS devices
• Algorithms and data structures
  C Computational Complexity, Big-O notation
  C NP-Completeness, Graph theory and data structures
• Circuit Partitioning
  C Kernighan-Lin algorithm
  C Fiduccia-Mattheyses algorithm
• Floorplanning
  C Representation using Normalized Polish Expression
  C Simulated Annealing Algorithm
  C Floorplanning using mathematical programming
• Placement
  C Simulated Annealing algorithm
  C Force directed placement
  C Partitioning based placement
  C Min-Cut placement, Terminal Propagation
• Routing
  C Global Routing: Steiner Trees
  C Global Routing: Lee’s algorithm
  C Global Routing: Soukup’s, Hadlock’s algorithm
  C Channel Routing: Left-edge algorithm
  C Channel Routing: VCG and HCG
  C Channel Routing: Constrained left-edge Doglog algorithm
• Trends in nano-scale IC design, transistor scaling

Outcome Assessments (Grades):
  Homework  45%
  Midterm    25%
  Final Exam 25%
  Class Participation 5%

Class Schedule:
  Class Twice a week for one hour and fifteen minutes.

Contribution of course to meeting the requirements of Criterion 5:
  3 credit hours of Engineering Topics and contains significant engineering design content

Relationship of course to student outcomes:
  b. An ability to design and conduct experiments, as well as to analyze and interpret data.
  c. An ability to design a system, component, or process to meet desired needs.
  e. An ability to identify, formulate, and solve engineering problems.
  k. An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice.

Instructor:
  Sanghamittra Roy, Assistant Professor
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