ECE 5470/6470

VLSI Design

Description: This course addresses advanced issues in VLSI design, covering the following topics: CMOS transistor theory, non-ideal effects in CMOS devices, design methodologies and IP design, CMOS circuit scaling, advanced logic circuit styles, noise sources and signal integrity in digital design, design techniques for dynamic and static power reduction, power supply issues, interconnect analysis, clocking and synchronization. The course also introduces the standard cell library based ASIC design flow. Students are expected to complete a substantial design project as part of the course, which involves extensive use of CAD tools.

Instructor: Dr. Sanghamitra Roy

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Lectures: TR 3.00pm-4.15pm, EL 109

Office hours: W 10.00am-11.00am (or by appointment)

Prerequisites: ECE 5460/6460

Textbook: Neil Weste and David Harris, **CMOS VLSI Design – A Circuits and Systems Perspective**, Fourth edition, Addison Wesley.

References (Optional):

- A. Chandrakasan, W. Bowhill, F. Fox, ***Design of High-Performance Microprocessor Circuits***, IEEE Press, 2000.
- Selected material from recent publications.

Course Webpage:
https://spaces.usu.edu/display/usuece5470/ECE+5470+VLSI+Design

Learning Objectives: By the end of the course, you should be able to do the following things:

1. *Synthesize*, and *place and route* industrial designs using commercial VLSI CAD tools.
2. *Analyze* the current, timing and power characteristics of CMOS circuits.
3. *Optimize* circuit designs for improving timing and power characteristics.
4. *Critique* circuit families for different applications.

Homework/Labs: There will be homework and/or lab assignments given approximately on a biweekly basis to help understand the concepts. Some of the homework assignments will involve programming and usage of CAD tools to familiarize students with CAD design flows. Students are expected to work 8 to 10 hours per week on the CAD tool assignments. We will use software tools installed in the VLSI Design Automation Lab machines. If you do not have accounts, please contact Scott Kimber to have accounts. The lab is reserved on Wednesday afternoons 12.30-4.30pm for this class. You can use the lab at other times also if available, or by remote login.

Computer Use: This course will involve several CAD tool assignments using the Synopsys and Cadence packages in the Design Automation lab.

Final Project: This course involves a substantial design project. The final project will be done in groups of two or three students. The instructor will provide a list of potential topics and resources, but teams will also be given freedom to propose their own topic. Teams are required to submit a proposal, a midterm progress report, a final report and all implementation files. Each

team will also prepare a presentation to demonstrate their results. **Project topic cannot be changed beyond two weeks after the proposal deadline.**

Exams: There will be one midterm exam. The exam will be open book and calculators will be allowed. Hand-held computers (PDAs) or laptops are not allowed.

Grading: The following weights will be used:

Homework and Labs: 30%
Midterm: 25%
Final project: 40%
Class participation: 5%

Grading is based on a conventional fixed scale:

A > 90%
A- > 85%
B+ > 80%
B > 70%
B- > 65%
C+ > 60%
C > 55%
C- > 50%
D+ > 47%
D > 44%
D- > 40%
F < 40%

The instructor reserves the right to curve up the scores at the end of the semester.

Late policy: Late submissions will not be accepted without prior approval by the instructor.

Disabilities: In cooperation with the Disability Resource Center, reasonable accommodation will be provided for qualified students with disabilities. Please meet with the instructor during the first week of class to discuss possible arrangements.

Cheating and Plagiarism: Cheating and plagiarism is not permitted. The instructor reserves the right to fail any student who is caught cheating and/or plagiarizing.

Course outline: The following topics will be covered with some variations.

1) CMOS Transistor Theory
2) Timing Verification
3) Clocking, synchronization & metastability
4) Dynamic power reduction
5) Low Leakage design
6) Interconnect & Inductance
7) CMOS Scaling
8) Circuit Design Styles

In addition, the following topics will be covered if time permits:

1) Electromigration reliability
2) Hot carrier reliability and NBTI
3) Noise sources, analysis
4) Testing of high-performance microprocessors
5) Asynchronous design
6) Packaging and Power Supply