ECE 5480/6480
VLSI Testing and Verification

Description: This course covers the theory and practice of testing and verification of VLSI systems. Topics span a broad range covering fault modeling, fault simulation, test generation, scan design and design for testability (DFT). Students get experience with commercial testing and DFT tools.

Instructor: Dr. Sanghamitra Roy

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Lectures: TR: 1.30-2.45PM, EL 109

Office hours: Wednesdays 10.00am-11.00am (or by appointment)

Prerequisites: ECE 2700 and Professional Program Status or Graduate Standing.

Textbook: Michael L. Bushnell and Vishwani D. Agrawal, Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits, Springer, Boston, 2005.

References:

- Selected material from recent publications.

Course Webpage:
https://spaces.usu.edu/display/ECE59306930/VLSI+Testing+and+Verification

Learning Objectives: By the end of the course, you should be able to do the following things:

1. *Model* and *simulate* different types of faults in digital circuits at the gate level.
2. *Establish* equivalence and dominance relationships of faults in a circuit.
3. *Critique* and *compare* automatic test pattern generation algorithms with respect to search space, speed, fault coverage and other criteria.

Homework and Labs: There will be homework and/or lab assignments every one to two weeks to help understand the concepts. These assignments will involve some use of the workstations in VLSI Design Automation lab. Tutorials will be provided for learning the software tools.

Exams: There will be a in-class midterm and a take-home final exam. These in-class exams will be closed book except for the use of one letter sized sheet (both sides) containing your own notes. Hand-held computers (PDAs) or laptops, cell phones are not allowed.

Additional Requirements for 6480 students: While all students will be doing a mini project involving generation of economical test and fault diagnosis in a test chip, the 6480 students will develop a tutorial guide for test generation and fault diagnosis using the Tetramax tool as an additional component.

Grading: The following weights will be used:

Homework and Labs: 45%
Midterm: 25%
Final exam: 25%
Class participation: 5%

Grading is based on a conventional fixed scale:

A: 90-100%
A-: 85-89%
B+: 80-84%
B: 70-79%

B-: 65-69%

C+: 60-64%

C: 55-59%

C-: 50-54%

D+: 47-49%

D: 44-46%

D-: 40-43%

F: 0-39%

The instructor reserves the right to curve up the scores at the end of the semester.

Late policy: Late submissions will not be accepted without prior approval by the instructor.

Disabilities: In cooperation with the Disability Resource Center, reasonable accommodation will be provided for qualified students with disabilities. Please meet with the instructor during the first week of class to discuss possible arrangements.

Cheating: Cheating or plagiarism is not permitted. The instructor reserves the right to fail any student who is caught cheating.

Course Outline: The following topics will be covered with some variations:

- Introduction, Test process and test equipment
- Test Economics
- Logic Modeling, Fault Modeling
- Logic and Fault Simulation
- Combinational test generation basics
- ATPG Algorithms: D-Algorithm, PODEM,FAN
- Testability Measure, ATPG systems
- Sequential Circuit ATPG
- Functional Testing: Checking Experiments

In addition, the following topics will be covered if time permits:

- Design for Testability (DFT)
- Built-In Self-Test
- Boundary Scan
- System Test
- Mixed Signal Testing